

IN THE DRAWINGS:

Please enter the attached corrected drawings Figs. 5A-H, in which reference "US" is being changed into "PS", to replace Figs. 5A-H as originally filed. A Letter to Draftsperson is also submitted herewith.

REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated March 23, 2006. In view of the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 2-6 and 9-10 are under consideration in this application. Claims 1 and 7-8 are being cancelled without prejudice or disclaimer. Claims 2 and 5 are being amended, as set forth in the above marked-up presentation of the claim amendments, in order to more particularly define and distinctly claim Applicants' invention. A new claim 10 is being added.

The claims and the drawings are being amended to correct formal errors and/or to better disclose or describe the features of the present invention as claimed. All the amendments to the specification and the claims are supported by the specification. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

Formality Rejection

The Title of the Invention was objected to as being non-descriptive. As indicated, the Title of the Invention is being amended as required by the Examiner. Accordingly, the withdrawal of the outstanding informality rejection is in order, and is therefore respectfully solicited.

Prior Art Rejections

Claims 1-2, 4-5 and 8-9 were rejected under 35 U.S.C. § 102(b) as being anticipated by JP 7-72508 to Konya et al. (hereinafter "Konya"), and claims 3 and 6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Konya in view of US Patent No. 6,356,331 B1 to Ono et al. (hereinafter "Ono '331") and US Application Pub. No. 2002/0047970 A1 of Ono et al. (hereinafter "Ono '970"). These rejections have been carefully considered, but are most respectfully traversed.

The display device of the invention (for example, the embodiment depicted in Fig. 1; pp. 8-15), as now recited in claims 2 and 10, comprises: signal lines DLs which are formed on an upper surface side of a substrate SUB1 to provide a display region AR (Fig. 2A); an insulation film IN which is formed such that the film covers the signal lines DLs except for terminal portions of the signal lines DLs in periphery of the substrate SUB1 (p. 12, 1st paragraph); and conductive layers MTs which extend in an extension direction of the signal lines DLs such that the conductive layers MTs traverse the terminal portions.

In claim 2, a pair of gaps are formed on respective sides of each of the conductive layers MTs parallel to the extension direction as well as between said each conductive layer MT and the insulation film IN, and a pair of holes HLs are formed in the signal lines DLs at portions underneath and corresponding to the pair of gaps along the extension direction (Fig. 1C). Each conductive layer MT is formed on the signal lines DLs and between the pair of holes HLs, while the insulated film IN is formed on the signal lines DLs and outside of the pair of holes HLs (Figs. 1A and 1C).

According to claim 10, each of the signal lines DL branches to three along the extended direction to provide a central portion and two side/edge portions on two sides of the main portion, and said each conductive layer MT is formed on the central portion, and the insulation film IN is formed on the side/edge portions (Figs. 1A and 1C).

Applicants respectfully contend that none of the cited references teaches or suggests that “each conductive layer MT is formed on the signal lines DLs and between the pair of holes HLs, while the insulated film IN is formed on the signal lines DLs and outside of the pair of holes HLs” as in the present invention.

In contrast, Konya’s terminal film 31a only branches to two (Fig. 6) to provide ONE hole, rather than a pair of holes as does the invention. In addition, the wiring layer 31b is formed on the branched terminal films 31a and broken by the hole 34, rather than formed between a pair of holes HLs as in the invention.

Moreover, Konya’s insulation layer 24 is formed above the signal lines DLs 31a with the wiring/conductive layer 31b or the insulation layer 12 in-between, rather than “directly on” the signal lines DLs 31a. Konya’s insulation layer 24 is simply not formed “outside of a pair of holes HLs.” As to the insulation layer 12, it is formed directly on the signal lines DLs 31a; however, there is NO gap between the insulation layer 12 and the wiring/conductive layer 31b. Konya’s insulation layer 12 is simply not formed “outside of a pair of holes HLs.”

The invention of claim 5 is directed to a display device (for example, the embodiment depicted in Fig. 6; pp. 22-25) comprising: signal lines DLs which are formed on an upper surface side of the substrate SUB1 to provide a display region AR; semiconductor layers PSs which are formed below the signal lines DLs by way of a first insulation film GI such that the semiconductor layers PSs traverse the signal lines DLs at terminal portions of the signal lines DLs in periphery of the substrate SUB1; a second insulation film IN which is formed on top of the substrate SUB1 to cover the signal lines DLs and in which holes HLs are formed above regions thereof where the semiconductor layers PSs are formed; conductive layers MTs which have respective sides thereof in the extension direction of the signal lines DLs arranged at both sides of the signal lines DLs and are connected with respective semiconductor layers PSs (Fig. 6C). The display region AR includes thin film transistors TFTs (Fig. 2), and a material of the semiconductor layers PSs in the periphery of the substrate SUB1 is equal to a material of semiconductor layers of the thin film transistors TFTs in the display region AR (original claim 7).

Konya's Fig. 13 was cited to cover the features of claim 5 (p. 3, last paragraph of the outstanding Office Action). However, Fig. 13 is a figure of the display region, rather than the periphery of the substrate SUB1 where the semiconductor layers PSs traverse the signal lines DLs at terminal portions of the signal lines DLs. As such, Konya does not teach the unique structure provided in the periphery of the substrate SUB1 as the present invention.

Ono '331 and Ono '970 were relied upon by the Examiner (p. 5, last paragraph and p. 6, first paragraph of the outstanding Office Action) to cover the features recited in claims 3 and 6. However, they fail to compensate for Konya's deficiencies as discussed above.

Applicant contends that Konya, Ono '331, and Ono '970 do not teach or disclose each and every feature of the present invention as disclosed in at least independent claims 1 and 5. As such, the present invention as now claimed is distinguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

Conclusion

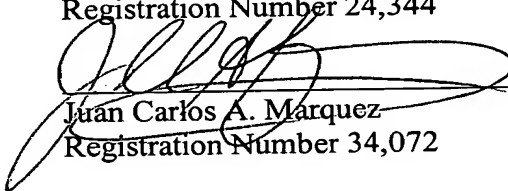
In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art references upon which the rejections in the

Office Action rely, Applicants respectfully contend that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicants' undersigned representative at the address and telephone number indicated below.

Respectfully submitted,

Stanley P. Fisher
Registration Number 24,344


Juan Carlos A. Marquez
Registration Number 34,072

REED SMITH LLP
3110 Fairview Park Drive
Suite 1400
Falls Church, Virginia 22042
(703) 641-4200

August 15, 2006

SPF/JCM/JT